CLAIMS

1. A magnetoresistive random access memory comprising:

a plurality of first wirings which is extended in a first direction;

a plurality of second wirings which is extended in a second direction which is substantially perpendicular to said first direction;

a plurality of memory cells, each of which is placed correspondingly to each of positions where said plurality of first wirings is crossed with said plurality of second wirings;

a second sense amplifier which detects a state of a reference cell on the basis of an output from said reference cell provided by corresponding to a reference wiring among said plurality of second wirings, among said plurality of memory cells; and

a first sense amplifier which detects a state of one of said plurality of memory cells on the basis of an output from said reference cell and an output from said one of the plurality of memory cells, which is different from said reference cell,

wherein each of said plurality of memory cells includes a magnetic tunneling junction element having a laminated free layer in which a magnetization direction is reversed correspondingly to data to be stored, and

wherein said magnetic tunneling junction element has a magnetization easy axis direction which is different from

said first and second directions.

2. The magnetoresistive random access memory according to claim 1, wherein a toggle operation to reverse a magnetization of said laminated free layer, for a selected cell as one of plurality of memory cells which corresponds to a selected first wiring selected among said plurality of first wirings and a selected second wiring selected among said plurality of second wirings, is executed by a series of current controls in which a first write current is supplied to said selected first wiring followed by a second write current to be supplied to said selected second wiring next, then, said first write current is stopped followed by said second write current to be stopped.

3. The magnetoresistive random access memory according to claim 2, wherein said first write current and said second write current are larger in said toggle operation executed for said reference cell than in said toggle operation executed for one of said plurality of memory cells which is different from said reference cell.

4. The magnetoresistive random access memory according to claim 2, wherein a stored information of said reference cell is read out by executing a first read-out operation to detect a first state as an initial state of said reference cell, a first toggle operation to bring said

reference cell into a second state by said toggle operation, a second read-out operation to detect said second state of said reference cell, and a second toggle operation to return said reference cell to said first state by said toggle operation, thereby stored information of the reference cell is read out on the basis of a comparison result between said first state and said second state.

5. The magnetoresistive random access memory according to claim 2, wherein a stored information of said reference cell is written by executing a first read-out operation to detect a first state as an initial state of said reference cell, a first toggle operation to bring said reference cell into a second state by said toggle operation, a second read-out operation to detect said second state of said reference cell, and a determination operation to determine said first state and said second state on the basis of a comparison result between said first state and said second state, thereby said second state is retained if said second state is equal to said stored information to be written to said reference cell, and said toggle operation is executed to return said reference cell to said first state if said second state is different from said stored information to be written to said reference cell, for writing.

6. The magnetoresistive random access memory according

to claim 4, wherein said second sense amplifier includes:

a resistance voltage converter which detects a resistance value of said magnetic tunneling junction element of said reference cell so as to convert to an output voltage,

a storage unit which temporarily stores said output voltage, and

a determination unit which determines said stored information which has been stored in said reference cell on the basis of said output voltage after said toggle operation and said output voltage before said toggle operation stored in said storage unit.

7. The magnetoresistive random access memory according to claim 6, wherein said storage unit includes:

a first switch unit which is connected to an output side of said resistance voltage converter at an input side, and

a capacitor which is connected to an output side of said first switch at an input side,

wherein said determination unit includes:

an inverter which is connected to an output side of the capacitor at an input side, and

a second switch unit which is connected in parallel between an input and said output of said inverter.

8. The magnetoresistive random access memory according

to claim 7, wherein both said first switch unit and said second switch unit are in an on state in said first read-out operation,

wherein said first switch unit is in an off state before starting said second read-out operation,

wherein said first switch unit is again brought into an on state immediately after said second switch unit is brought into an off state in said second read-out operation, and

wherein an output of said inverter in said second read-out operation is said stored information of said reference cell.

9. The magnetoresistive random access memory according to claim 4, wherein said second sense amplifier detects whether or not said first toggle operation is executed, and increases said first write current and said second write current if it is determined that said first toggle operation is not executed to start from said first read-out operation again.

10. The magnetoresistive random access memory according to claim 9, wherein said second sense amplifier includes:

a first resistance voltage converter which detects a resistance value of said magnetic tunneling junction element of said reference cell as a first output voltage,

a first storage unit which temporarily stores said

first output voltage,

a first determination unit which determines said stored information stored in said reference cell and outputs a determination result as a first signal on the basis of said first output voltage after said toggle operation and said first output voltage before said toggle operation stored in said first storage unit,

a second resistance voltage converter which detects a resistance value of said magnetic tunneling junction element of said reference cell as a second output voltage,

a second storage unit which temporarily stores said second output voltage,

a second determination unit which determines said stored information stored in said reference cell and outputs a determination result as a second signal on the basis of said second output voltage after said toggle operation and said second output voltage before said toggle operation stored in said second storage unit, and

a determination unit which determines whether or not said first toggle operation has been executed on the basis of said first signal and said second signal.

11. The magnetoresistive random access memory according to claim 10, wherein said first output voltage in said first read-out operation is obtained by adding a first offset voltage to a voltage to which a detected resistance value of said magnetic tunneling junction element is converted,

wherein said first output voltage in said second read-out operation is obtained by detecting a resistance value of said magnetic tunneling junction element and converting it to a voltage,

wherein said second output voltage in said first read-out operation is obtained by adding a second offset voltage to a voltage to which a detected resistance value of said magnetic tunneling junction element is converted,

wherein said second output voltage in said second read-out operation is obtained by detecting a resistance value of said magnetic tunneling junction element and converting it to a voltage, and

wherein a sign of said first offset voltage is opposite to that of said second offset voltage.

12. The magnetoresistive random access memory according to claim 10, wherein said first output voltage in said first read-out operation is obtained by adding a first offset voltage to a voltage to which a detected resistance value of said magnetic tunneling junction element has been converted,

wherein said first output voltage in said second read-out operation is obtained by detecting a resistance value of the magnetic tunneling junction element and converting it to a voltage,

wherein said second output voltage in said first read-out operation is obtained by detecting a resistance

value of said magnetic tunneling junction element and converting it to a voltage,

wherein said second output voltage in said second read-out operation is obtained by adding a second offset voltage to a voltage to which a detected resistance value of said magnetic tunneling junction element has been converted, and

wherein a sign of said first offset voltage is equal to that of said second offset voltage.

13. The magnetoresistive random access memory according to claim 11, wherein said first storage unit includes:

a first switch unit which is connected to an output side of said first resistance voltage converter at an input side, and

a first capacitor which is connected to an output side of said first switch unit at an input side,

wherein said first determination unit includes:

a first inverter which is connected to an output side of said first capacitor at an input side, and

a second switch unit which is connected in parallel between an input and an output of said first inverter,

wherein said second storage unit includes:

a third switch unit which is connected to an output side of said first resistance voltage converter at an input side, and

a second capacitor which is connected to an output

side of said third switch at an input side,

wherein said second determination unit includes:

a second inverter which is connected to an output side of the second capacitor at an input side, and

a forth switch unit which is connected in parallel between an input and an output of said second inverter.

14. The magnetoresistive random access memory according to claim 13, wherein said first switch unit, said second switch unit, said third switch unit and said forth switch unit are in an on state in said first read-out operation,

wherein said first switch unit and said third switch unit are in an off state before starting the second read-out operation,

wherein said first switch unit and said third switch unit are brought into an on state again immediately after said second switch unit and said fourth switch unit are brought into an off state in said second read-out operation, and

wherein an output of said determination unit in said second read-out operation is said stored information of said reference cell.